IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

REVOCATION OF POWER OF ATTORNEY

Assistant Commissioner for Patents Alexandria, VA 22313-1450

Dear Sir:

I am an officer of <u>MACRONIX International Co., Ltd.</u> authorized to act on behalf of <u>MACRONIX International Co., Ltd.</u>, the assignee of the entire right, title and interest in the attached list of applications for patent. Evidences of these assignments are recorded in the Patent and Trademark Office as the enclosed list, Appendix A.

. I hereby revoke all previous powers of attorney to prosecute these applications and to transact all business connected therewith.

POWER OF ATTONEY

As an officer of the assignee of the entire right, title and interest in the above-referenced application for patent, I hereby appoint the following attorney(s) and/or Agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Belinda Lee

(Reg. No. 46,863)

SEND CORRESPONDENCE TO:

DIRECT TELEPHONE CALLS TO:

(Name and Telephone Number)

Belinda Lee

JIANQ CHYUN Intellectual Property Office

7F.-1, No. 100, Roosevelt Rd., Sec. 2,

Taipei 100, Taiwan, R.O.C.

TEL: 886-2-2369 2800 FAX: 886-2-2369 7233

E-mail: Belinda@JCIPGroup.com.tw; USA@JCIPGroup.com.tw

CHIH YUAN LU

President

MACRONIX International Co., Ltd.

METHOD FOR ELININATIONG POLYCIDE VOIDS THROUGH 2005/IL28 I.1044,212 016047 10311-US-PA NITROGEN IMPLANTATION 2005/IL28 I.10600700 014223 10496-US-PA PVCS (PEER VERSION CONTROL SYSTEM) 2003/IC219 10/731150 014785 APPARATUS AND METHOD USING OZONE DI PROCESS 2003/IC219 10/731150 014785 AND TEST MODE TO SCREEN MARGINAL CELLS IN AN NROM AND TEST MODE TO SCREEN MARGINAL CELLS IN AN NROM 11/096,878 016092 AND TEST MODE TO SCREEN MARGINAL CELLS IN AN NROM 2005/4/11 11/096,878 016359 AND TEST MODE TO SCREEN MARGINAL CELLS IN AN NROM 2005/4/11 11/096,878 017235 AND TEST MODE TO SCREEN MARGINAL CELLS IN AN NROM 2007/9/17 11/856,457 016359 AND TEST MODE TO FORMING ONO FOR NITRIDE FLASH MEMORY 2007/9/19 11/964,322 017235 AND TEST MON-VOLATILE MEMORY 2005/IL/15 11/735,360 017835 AND TEST MODE TO FORMING ONO FOR NITRIDE FLASH MEMORY 2005/IL/15 11/385,360 017835 AND TEST METHOD TO FORM MEMORY 2005/IL/15 11/385,360 017835 AND TEST METHOD SOF TRENCH AND CONTACT FORMATION IN MEMORY 2005/IL/15 11/385,360 017835 AND TEST METHOD SOF TRENCH AND CONTACT FORMATION IN MEMORY 2005/IL/15 11/385,360 017835 AND TEST METHOD SOF TRENCH AND CONTACT FORMATION IN MEMORY 2005/IL/15 11/385,360 017835 AND TEST METHOD SOF TRENCH AND CONTACT FORMATION IN MEMORY 2005/IL/15 11/385,360 017835 AND TEST METHOD SOF TRENCH AND CONTACT FORMATION IN MEMORY 2005/IL/15 20	fat Gaza	Attorney Docket No.	TITLE	Filing Date	Appl. No.	Reel No.	Frame No.
10311-US-PA NITROGEN IMPLANTATION 2003/6/23 11/044,212 10496-US-PA PVCS (PEER VERSION CONTROL SYSTEM) 2003/6/23 10/600700 11064-US-PA CLEANING METHOD USING OZONE DI PROCESS 2003/12/10 10/731150 11064-US-PA APPARATUS AND METHOD TO IMPROVE THE ERASE UNIFORMITY 2003/12/10 10/731150 1474-US-PA AND TEST MODE TO SCREEN MARGINAL CELLS IN AN NROM 2005/4/1 11/096,878 14994-US-PA MEMORY ARRAY 2007/9/1 11/856,457 15319-US-PA METHOD OF FORMING ONO FOR NITRIDE FLASH MEMORY 2007/9/1 11/364,322 METHOD OF FORMING ONO FOR NITRIDE FLASH MEMORY 2007/9/1 11/364,322 METHOD TO FORM ONO AND DIFFUSION BIT LINES FOR NITRIDE 2005/4/1 11/385,360 15720-US-PA THREE-DIMENSIONAL MEMORY 2005/3/2 11/385,360 15720-US-PA THREE-DIMENSIONAL MEMORY 2006/7/26 11/459,990 16732-US-PA METHODS OF TRENCH AND CONTACT FORMATION IN MEMORY 2006/7/26 11/459,990			METHOD FOR ELININATIONG POLYCIDE VOIDS THROUGH				
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11064-US-PA CLEANING METHOD USING OZONE DI PROCESS 2003/12/10 10/731150 APPARATUS AND METHOD TO IMPROVE THE ERASE UNIFORMITY AND TEST MODE TO SCREEN MARGINAL CELLS IN AN NROM 2005/4/1 11/096,878 14744-US-PA MEMORY ARRAY 2007/9/17 11/856,457 15319-US-PA METHOD OF FORMING ONO FOR NITRIDE FLASH MEMORY 2007/9/17 11/856,457 15319-US-PA-I METHOD OF FORMING ONO FOR NITRIDE FLASH MEMORY 2007/9/19 11/964,322 15706-US-PA THREE-DIMENSIONAL MEMORY DEVICES 2006/3/21 11/385,360 15720-US-PA THREE-DIMENSIONAL MEMORY DEVICES 2006/3/21 11/385,360 15937-US-PA CELLS CELLS CELLS CELLS CELLS 1694-US-PA METHOD OF TRENCH AND CONTACT FORMATION IN MEMORY 2006/3/21 11/385,360 15937-US-PA CELLS CELLS CELLS CELLS CELLS 11/459,990 15937-US-PA CELLS CELLS CELLS CELLS CELLS 11/499-US-PA CELLS CELLS CELLS CELLS CELLS 11/499-US-PA CELLS CELLS CELLS CELLS 11/499-US-PA CELLS CELLS CELLS CELLS CELLS 11/499-US-PA CELLS CELLS CELLS CELLS 11/499-US-PA CELLS CELLS CELLS CELLS CELLS 11/499-US-PA CELLS CELLS CELLS 11/499-US-PA CELLS CELLS CELLS CELLS 11/499-US-PA CELLS CELLS CELLS 11/499-US-PA CELLS CELLS CELLS CELLS 11/499-US-PA CELLS 11/499-US-	2	10496-US-PA	PVCS (PEER VERSION CONTROL SYSTEM)	2003/6/23	10/600700	014223	0556
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14994-US-PA ARRAY 2007/9/17 11/856,457 15319-US-PA METHOD OF FORMING ONO FOR NITRIDE FLASH MEMORY 2005/11/15 11/274,781 15319-US-PA-1 METHOD OF FORMING ONO FOR NITRIDE FLASH MEMORY 2007/9/19 11/964,322 METHOD TO FORM ONO AND DIFFUSION BIT LINES FOR NITRIDE 2005/8/23 11/209,875 15706-US-PA NON-VOLATILE MEMORY 2005/8/23 11/209,875 15720-US-PA THREE-DIMENSIONAL MEMORY DEVICES 2006/3/21 11/385,360 METHODS OF TRENCH AND CONTACT FORMATION IN MEMORY 2006/7/26 11/459,990			OPERATION METHODS FOR A NON-VOLATILE MEMORY CELL IN AN				
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15706-US-PA NON-VOLATILE MEMORY 2005/8/23 11/209,875 15720-US-PA THREE-DIMENSIONAL MEMORY DEVICES 2006/3/21 11/385,360 METHODS OF TRENCH AND CONTACT FORMATION IN MEMORY METHODS OF TRENCH AND CONTACT FORMATION IN MEMORY 2006/7/26 11/459,990			METHOD TO FORM ONO AND DIFFUSION BIT LINES FOR NITRIDE				
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METHODS OF TRENCH AND CONTACT FORMATION IN MEMORY 15937-US-PA CELLS 2006/7/26 11/459,990	6	15720-US-PA		2006/3/21	11/385,360	017832	6890
15937-US-PA CELLS CELLS 11/459,990							
	2		CELLS	2006/7/26	11/459,990	018386	0511



	Attorney Docket No.	TITLE	Filing Date	Appl. No.	Reel No.	Frame No.
		A PARTIAL SILICON-ON-INSULATOR STRUCTURE AND ITS				
=	15954-US-PA	FABRICATION METHOD	2006/5/18	11/383,973	018038	7620
		NON-VOLATILE MEMORY CELLS AND METHODS OF				
12	15962-US-PA	MANUFACTURING THE SAME	2005/8/4	11/197,659	016520	0672
13	15963-US-PA	DIODE-LESS ARRAY FOR ONE-TIME PROGRAMMABLE MEMORY	2005/12/8	11/297,529	018067	0737
		METHOD OF MANUFACTURING DUAL GATE MULTI-BIT				
		SEMICONDUCTOR MEMORY BY USING POLYMER SHRINKED				
14	16279-US-PA	NANO-SPACE	2006/2/13	11/352,788	019284	9620
15	16343-US-PA	A METHOD TO PRODUCE HIGH VOLTAGE DEVICE	2005/12/16	11/303.176	017368	0066
16	16 16646-US-PA	DUAL GATE MULTI-BIT SEMICONDUCTOR MEMORY	2006/2/17	1	017481	960
17	17610-US-PA	METHOD OF RESOLUTION IMPROVEMENT	2006/6/5	11/422,284	018060	0504
		PATTERN REGISTRATION MARK DESIGNS FOR USE IN				
81	17845-US-PA	PHOTOLITHOGRAPHY AND METHODS OF USING THE SAME	2006/4/25	11/410,424	017837	0553
19	19109-US-PA	A SYSTEM FOR OPERATING A MEMORY DEVICE	2008/3/21	12/053,411	020686	0153
20	19110-US-PA	DECODING METHOD IN AN NROM FLASH MEMORY ARRAY	2006/9/25	11/534,696		

	Attorney Docket No.	Title	Filing Date	Appl. No.	Reel No.	Frame No.
	-	A Semiconductor Structure And Process For Reducing The Second Bit Effect Of				And the second s
21	19681-US-PA	A Memory Device	2007/4/10	11/786,078	019446	0496
22	21044-US-PA	A Method To Increase Gcr Of Virtual Ground Floating Gate Flash Memories	2006/5/12	11/383,073	017611	0588
	-	Structure Of Magnetic Random Access Memory Using Spin-Torque Transfer				
23	21247-US-PA	Writing And Method For Manufacturing Same	2006/12/1	11/607,612	018734	6110
	-	Cell Operation Methods Using Gate-Injection For Floating Gate Nand Flash				
24	21370-US-PA	Memory	2006/10/3	11/542,749	018651	8650
25	21566-US-PA	Side Lobe Image Searching Method In Lithography	2006/12/28	11/647,068	018885	0386
		Spatial Energy Distribution By Slit Filter For Step-And-Scan System On				
26	21567-US-PA	Multiple Focus Exposure	2007/1/4	11/649,570	020122	0220
27	21706-US-PA	Resistance Random Access Memory	2007/1/19	11/656,246	019032	0600
		A Non-Volatile Semiconductor Memory Device And A Method Of Fabricating				
28	21707-US-PA	A Nonvolatile Semiconductor Memory Device	2007/3/30	11/693,716	019095	0943
		Inverted T-Shaped Floating Gate Memory And Method For Fabricating The				
29	21830-US-PA	Same	2008/2/22	12/036,196	020553	0422
		Method Of Programming And Erasing A P-Channel Be-Sonos Nand Flash				
30	30 27491-US-PA	Memory	2006/5/5	11/381,760	186/10	0223

Attorney Docket No							
27645-US-PA LOADING DATA WITH ERROR DETECTION IN A POWER ON 2006/10/5 11/538,844 018872 27826-US-PA SEQUENCE OF FLASH MEMORY DEVICE 2006/12/27 11/538,844 018872 27826-US-PA-0C PROCESS 2006/12/27 11/646,205 020713 27829-US-PA DOUBLE EXPOSURE APPLICATION 2006/12/27 11/017,684 016123 27830-US-PA METHOD OF FORMING BOTTOM OXIDE FOR NITRIDE FLASH 2006/12/27 11/017,684 016123 27831-US-PA MEMORY 2005/9/27 11/235,786 016754 27832-US-PA ASYMMETRIC FLOATING GATE NAND FLASH MEMORY 2005/9/27 11/293,888 016826 27833-US-PA THE REFERENCE CELLS AUTO TRIMMING 2005/11/10 11/21/3,08 016968 27833-US-PA ARRAY WORD LINE ANOVEL DOPING PROFILE TO IMPROVE THE INTEGRITY OF TWIN 2005/9/27 11/209,145 017370 27834-US-PA BIT CELL FLASH MEMORY 2005/9/27 11/209,145 017370 27835-US-PA BIT CELL FLASH MEMORY 2005/9/15 11/203,148 017370			TITLE	Filing Date	Appl. No.	Reel No.	Frame No:
27645-US-PA SEQUENCE OF FLASH MEMORY DEVICE 2006/10/5 11/538,844 018872 27826-US-PA-0C NEURAL NETWORK FOR DETERMINING AN ENDPOINT IN AN ETCH 2006/12/27 11/646,205 020713 27826-US-PA-0C PROCESS DOUBLE EXPOSURE APPLICATION 2004/12/22 11/017,684 016123 27829-US-PA METHOD OF FORMING BOTTOM OXIDE FOR NITRIDE FLASH 2005/9/27 11/235,786 016754 27830-US-PA MEMORY 2005/9/27 11/235,786 016754 27831-US-PA ASYMMETRIC FLOATING GATE NAND FLASH MEMORY 2005/9/27 11/209,437 020871 27833-US-PA THE REFERENCE CELLS AUTO TRIMMING 2005/9/27 11/209,437 016968 27833-US-PA THE REFERENCE CELLS AUTO TRIMMING 2005/9/27 11/137,098 016968 27834-US-PA ARRAY WORD LINE ARRAY WORD LINE ANOVEL DOPING PROFILE TO IMPROVE THE INTEGRITY OF TWIN 2005/9/27 11/137,098 016309 27835-US-PA BIT CELL FLASH MEMORY 2005/9/15 11/209,145 017370 27836-US-PA MAP (MOBILE AUDIO PLATFORM) SYSTEM ARCHITECTURE 2005/9/15 11/20			LOADING DATA WITH ERROR DETECTION IN A POWER ON			TO THE PROPERTY OF THE PROPERT	
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27826-US-PA PROCESS 2006/12/27 11/646,205 020713 27829-US-PA DOUBLE EXPOSURE APPLICATION 2004/12/22 11/017,684 016123 27829-US-PA METHOD OF FORMING BOTTOM OXIDE FOR NITRIDE FLASH 2005/9/27 11/235,786 016754 27830-US-PA MEMORY 2005/9/27 11/235,786 016754 27831-US-PA ASYMMETRIC FLOATING GATE NAND FLASH MEMORY 2005/9/27 11/209,437 020871 27833-US-PA LOW-K SPACER STRUCTURE FOR THE FLASH MEMORY 2007/11/9 11/943,888 016368 27833-US-PA THE REFERENCE CELLS AUTO TRIMMING 2005/11/10 11/271,300 016968 27833-US-PA ARRAY WORD LINE ARRAY WORD LINE 11/271,300 11/271,300 016968 27835-US-PA BIT CELL FLASH MEMORY 2005/5/25 11/137,098 016302 27835-US-PA BIT CELL FLASH MEMORY 2005/9/15 11/209,145 017370 27835-US-PA MAP (MOBILE AUDIO PLATFORM) SYSTEM ARCHITECTURE 2005/9/15 11/227,380 016859			NEURAL NETWORK FOR DETERMINING AN ENDPOINT IN AN ETCH				
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27830-US-PA METHOD OF FORMING BOTTOM OXIDE FOR NITRIDE FLASH 2005/927 11/235,786 016754 27831-US-PA ASYMMETRIC FLOATING GATE NAND FLASH MEMORY 2005/8/23 11/209,437 020871 27832-US-PA LOW-K SPACER STRUCTURE FOR THE FLASH MEMORY 2007/11/9 11/943,888 016826 27833-US-PA THE REFERENCE CELLS AUTO TRIMMING 2005/11/10 11/271,300 016968 27834-US-PA ARRAY WORD LINE DRIVER WIDTH IS PERPENDICULAR TO 2005/5/25 11/137,098 016292 A NOVEL DOPING PROFILE TO IMPROVE THE INTEGRITY OF TWIN A NOVEL LEASH MEMORY 2005/8/22 11/209,145 017370 27836-US-PA MAPP (MOBILE AUDIO PLATFORM) SYSTEM ARCHITECTURE 2005/9/15 11/227,380 016859	33	- 1	DOUBLE EXPOSURE APPLICATION	2004/12/22	11/017,684	016123	0255
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27832-US-PA LOW-K SPACER STRUCTURE FOR THE FLASH MEMORY 2007/11/9 11/943,888 016826 27833-US-PA THE REFERENCE CELLS AUTO TRIMMING 2005/11/10 11/271,300 016968 27834-US-PA ARRAY WORD LINE ARRAY WORD LINE 2005/5/25 11/137,098 016292 27835-US-PA BIT CELL FLASH MEMORY 2005/8/22 11/209,145 017370 27836-US-PA MAP (MOBILE AUDIO PLATFORM) SYSTEM ARCHITECTURE 2005/9/15 11/227,380 016859	35		ASYMMETRIC FLOATING GATE NAND FLASH MEMORY	2005/8/23	11/209,437		0561
27833-US-PA THE REFERENCE CELLS AUTO TRIMMING 2005/11/10 11/271,300 016968 27834-US-PA ARRAY WORD LINE 2005/5/25 11/137,098 016292 27835-US-PA BIT CELL FLASH MEMORY 2005/8/22 11/209,145 017370 27835-US-PA MAP (MOBILE AUDIO PLATFORM) SYSTEM ARCHITECTURE 2005/9/15 11/227,380 016859	36		LOW-K SPACER STRUCTURE FOR THE FLASH MEMORY	2007/11/9	11/943,888	016826	1.00
27834-US-PA ARRAY WORD LINE DRIVER WIDTH IS PERPENDICULAR TO 2005/5/25 11/137,098 016292 27835-US-PA A NOVEL DOPING PROFILE TO IMPROVE THE INTEGRITY OF TWIN 2005/8/22 11/209,145 017370 27835-US-PA BIT CELL FLASH MEMORY 2005/8/22 11/227,380 016859	37	27833-US-PA		2005/11/10	11/271,300	016968	0287
27834-US-PA ARRAY WORD LINE 2005/5/25 11/137,098 016292 27835-US-PA BIT CELL FLASH MEMORY 2005/8/22 11/209,145 017370 27836-US-PA MAP (MOBILE AUDIO PLATFORM) SYSTEM ARCHITECTURE 2005/9/15 11/227,380 016859			LAYOUT OF WORD LINE DRIVER WIDTH IS PERPENDICULAR TO				
A NOVEL DOPING PROFILE TO IMPROVE THE INTEGRITY OF TWIN 27835-US-PA BIT CELL FLASH MEMORY 27836-US-PA MAP (MOBILE AUDIO PLATFORM) SYSTEM ARCHITECTURE 2005/9/15 11/227,380 016859	38	1	ARRAY WORD LINE	2005/5/25	11/137,098	016292	0235
27835-US-PA BIT CELL FLASH MEMORY 2005/8/22 11/209,145 017370 27836-US-PA MAP (MOBILE AUDIO PLATFORM) SYSTEM ARCHITECTURE 2005/9/15 11/227,380 016859			A NOVEL DOPING PROFILE TO IMPROVE THE INTEGRITY OF TWIN				
27836-US-PA MAP (MOBILE AUDIO PLATFORM) SYSTEM ARCHITECTURE 2005/9/15 11/227,380 016859	39		BIT CELL FLASH MEMORY	2005/8/22	11/209,145	017370	0912
	40	27836-US-PA	MAP (MOBILE AUDIO PLATFORM) SYSTEM ARCHITECTURE	2005/9/15	11/227,380	016859	0311

	Attorney Docket No.	TITLE	Tiling Date	Filing Date: Appl. No.	Reel No.	Frame No.
		METHOD OF FORMING AND OPERATING AN ASSISTED CHARGED		Photographic Action Control of the C		
41	27837-US-PA	NITRIDE-TRAP MEMORY DEVICE	2005/12/2	11/292,024	017249	0736
		NEGATIVE CHARGE-PUMP WITH CIRCUIT TO ELIMINATE PARASITIC				
42	27838-US-PA	DIODE TURN-ON	2005/9/23	11/233,901	016775	0633
		A LAYER DECODING SCHEME AND STRUCTURE FOR 3				
43	27839-US-PA	DIMENSIONAL MEMORY	2006/3/21	11/385,061	017568	0352
44	27840-US-PA	MAP (MOBILE AUDIO PLATFORM) DOWNLOAD SCHEME	2005/9/15	11/226,987	016838	0129
45	27841-US-PA	BACKGROUND SOUND MIXER	2005/9/15	11/227,621	016842	0445
		INTERFACE FOR A REMOVABLE ELECTRONIC DEVICE AND METHOD				
46	46 27842-US-PA	THEREOF	2005/9/15	11/227,622	016838	0554
47	27843-US-PA	METHOD FOR REFRESHING A FLASH MEMORY	2006/6/8	11/449,361	018152	0268
		METHODS OF ETCHING STACKS HAVING METAL LAYERS AND				
48	27844-US-PA	HARD MASK LAYERS	2006/5/9	11/382,401	017974	0192
		PLASMA ETCHING METHODS USING NITROGEN MEMORY SPECIES				
49	27845-US-PA	FOR SUSTAINING GLOW DISCHARGE	2006/2/22	11/359,787	017881	0520
20	27846-US-PA	PRESSURE CALIBRATION	2006/4/21	11/409,127	017806	0648

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		NON-VOLATILE MEMORY CELLS HAVING A				
		POLYSILICON-CONTAINING, MULTI-LAYER INSULATING STRUCTURE,				
		MEMORY ARRAYS INCLUDING THE SAME AND METHODS OF				-
51	27847-US-PA	OPERATING THE SAME	2006/10/27	11/588,830	018730	0493
		NVM CELLS HAVING OXIDE/NITRIDE MULTI-LAYER INSULATING		-		
52	27848-US-PA	STRUCTURES AND METHODS OF OPERATING THE SAME	2007/1/3	11/649,348	019275	1990
		A HIGH SECOND BIT OPERATION WINDOW METHOD FOR NAND				
53	27850-US-PA	ARRAY WITH TWO-BIT MEMORY CELLS	2008/2/22	12/035,786	020548	8800
	ē	METHOD OF IMPROVING OVERLAY PERFORMANCE IN				
54	27851-US-PA	SEMICONDUCTOR MANUFACTURE	2006/12/11	11/636,927	018707	0922
1						
55	27852-US-PA	FLASH MEMORY ARRAY ARCHITECTURE	2008/1/4	11/969,812	020703	1860
56	27853-US-PA	PROGRAMMING SCHEME FOR NON-VOLATILE FLASH MEMORY	2006/12/11	11/636,920	018833	0415
57	27854-US-PA	MEMORY SYSTEM AND A VOLTAGE REGULATOR	2007/3/30	11/693,712	019088	0615
		FLASH MEMORY WITH 4-BIT MEMORY CELL AND METHOD FOR				
58	27855-US-PA	FABRICATING THE SAME	2007/6/8	11/760,646	819610	1560
59	27856-US-PA	NON-VOLATILE MEMORY WITH IMPROVED ERASING OPERATION	7/2/1200	11/703,916	018983	0446
09	27857-US-PA	MEMORY CHIP WITH WRITE LOCK-DOWN FEATURE	2007/9/28	11/863,254	019893	0119

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19	27858-US-PA	MULTI-LEVEL-CELL TRAPPING DRAM	2007/6/11	4	020285	0331
<u> </u>		INVERTED T-SHAPED FLOATING GATE MEMORY AND METHOD FOR				
62	27859-US-PA	FABRICATING THE SAME	2007/11/16 11/941,813	11/941,813	020128	0727
63	27861-US-PA	METHOD FOR PERFORMING OPERATIONS ON A MEMORY CELL	2007/11/22	11/945,181	020154	0578
		METHOD OF FABRICATING INTEGRATED CIRCUIT WITH SMALL				
64	64 27863-US-PA	PITCH	2007/8/29	11/846,900	019762	0485
		PATTERNING STRUCTURE AND METHOD FOR SEMICONDUCTOR				
65	27864-US-PA	DEVICES	2007/11/21	11/943,900	020146	9/10
		A MASK FOR CONTROLLING LINE END SHORTENING AND CORNER				
99	27866-US-PA	ROUNDING ARISING FROM PROXIMITY EFFECTS	2008/1/9	11/971,900	020350	0108
29	21938-US-PA	MEMORY DEVICES	2008/6/13	12/139,418	021097	0746
		METHOD AND SYSTEM FOR MANUFACTRUING OPENING ON				
89	27867-US-PA	SEMICONDUCTOR DEVICES	2008/6/20	12/143,730	021132	0465
		TWO-BITS PER CELL NOT-AND GATE (NAND) NITRIDE TRAP				
69	28720-US-PA	MEMORY	2008/5/19	12/123,302	919910	0338